## REMARKS

Claims 1, 5-8, 11-16, 19-22, 35 and 38-40 have been amended. Claims 1-23, 35 and 38-41 are currently pending in this application. Applicants reserve the right to pursue the original and other claims in this and other applications. Applicants respectfully request reconsideration of the application in light of the amendments and the following remarks.

The Specification has been amended to correct typographical errors.

Claims 1-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lam (U.S. Patent No. 6,344,104) ("Lam"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 1 recites a method of making semiconductor device packages including "forming a plurality of conductive traces in contact with a top surface of an integral dielectric substrate, the plurality of conductive traces being located on said substrate in correspondence with a plurality of semiconductor devices in a wafer," "subsequently, forming a layered assembly by attaching said wafer to said integral dielectric substrate, such that said plurality of conductive traces are in electrical communication with said plurality of semiconductor devices in said wafer," "forming input/output devices in contact with said conductive traces," "testing semiconductor devices in said wafer," and "subsequently, dicing said layered assembly."

Claim 11 recites a method of making semiconductor device packages including "providing a plurality of conductive structures in contact with a top surface of an integral dielectric substrate, the plurality of conductive structures being located on said substrate in correspondence with a plurality of semiconductor devices in a semiconductor wafer," "subsequently, forming a layered assembly by attaching said

semiconductor wafer and a stiff metal layer to said integral dielectric substrate with said conductive structures electrically connecting with said semiconductor devices," "placing ball grid arrays in contact with said conductive structures," "electrically connecting said plurality of semiconductor devices in said semiconductor wafer to said ball grid arrays," "determining whether said semiconductor wafer contains a defective semiconductor device," and "subsequently, dicing said layered assembly."

Lam relates to a wafer level packaging method which produces a stacked dual/multiple die integrated circuit package by attaching individual dies from a first wafer to individual dies on a second wafer and then singulating the second wafer to form the individual stacked-die IC packages. (Abstract). Lam does not disclose, teach or suggest "forming a layered assembly by attaching [a] wafer to [an] integral dielectric substrate, such that [a] plurality of conductive traces are in electrical communication with [a] plurality of semiconductor devices in said wafer" as recited in claim 1 or "forming a layered assembly by attaching [a] semiconductor wafer and a stiff metal layer to [an] integral dielectric substrate" as recited in claim 11. Instead, Lam discloses attaching separate and individual (i.e. already singulated) dies to the surface of a second wafer. These individual dies do not disclose, teach or suggest an "integral dielectric substrate" as in the claimed invention.

Accordingly, Applicants respectfully submit that claims 1 and 11 are allowable over Lam. Claims 2-10 depend from claim 1 and are allowable along with claim 1. Claims 12-18 depend from claim 11 and are allowable along with claim 11. Applicants respectfully request that the rejection of claims 1-18 be withdrawn and the claims allowed.

Claims 19, 39 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoon et al. (U.S. Patent No. 6,479,887) ("Yoon") in view of Yang

(U.S. Patent No. 6,498,387) ("Yang"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 19 recites a method of making semiconductor device packages including "simultaneously aligning a plurality of semiconductor devices in a semiconductor wafer with respect to a plurality of pre-existing openings in a dielectric tape, before attaching said semiconductor wafer to said dielectric tape," "subsequently, attaching said semiconductor wafer to said dielectric tape," "connecting said semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric tape," and "simultaneously dicing said semiconductor wafer and said dielectric tape."

Yoon relates to a method of forming chip size semiconductor packages using a circuit pattern tape. As admitted by the Office Action, Yoon does not disclose aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape. (Office Action, pg. 5). The Office Action relies on Yang for this disclosure.

Yang relates to a wafer level package and the processing of the wafer level package. Yang discloses the steps of coating a wafer with an adhesive material, curing to harden the adhesive material, and forming a plurality of pad openings in the adhesive material that are aligned to the pads of the dies. (Yang, col. 3, lines 53-66). Applicants respectfully submit that Yang does not disclose "simultaneously aligning a plurality of semiconductor devices in a semiconductor wafer with respect to a plurality of pre-existing openings in a dielectric tape, before attaching said semiconductor wafer to said dielectric tape" as recited in amended claim 19. (emphasis added). Instead, Yang discloses a method of wafer level packaging wherein openings are formed in the adhesive material after it has been attached to the wafer. Therefore, the openings are not "pre-existing" and cannot be "simultaneously align[ed] ... before attaching said

semiconductor wafer to said dielectric tape" because the openings do not exist during attachment.

Accordingly, Applicants respectfully submit that claim 19 is allowable over the cited combination. Claims 39 and 40 depend from claim 19 and are allowable as well. Applicants respectfully request that the rejection of claims 19, 39 and 40 be withdrawn and the claims allowed.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoon in view of Yang and further in view of Gaynes et al. (U.S. Patent No. 6,165,885) ("Gaynes"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 20 depends from claim 19. Claim 19 is allowable over the combination of Yoon and Yang for at least the reasons discussed above. Gaynes is relied upon as disclosing the wafer being optically aligned with respect to the dielectric tape. (Office Action, pg. 6). Gaynes does not remedy the deficiencies of Yoon and Yang with respect to claim 19. Accordingly, Applicants respectfully submit that claim 19, and therefore claim 20, is allowable over the cited combination. Applicants respectfully request that the rejection of claim 20 be withdrawn and the claim allowed.

Claims 21-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoon in view of Yang and further in view of Smith (U.S. Patent No. 6,300,149) ("Smith"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claims 21-23 depend from claim 19. Claim 19 is allowable over the combination of Yoon and Yang for at least the reasons discussed above. Smith is relied upon as disclosing the wafer being magnetically aligned with respect to the dielectric

tape, oppositely charged magnetic elements being provided on the wafer and the dielectric tape, and locating a magnetic ring in a charge slot. (Office Action, pg. 6). Smith does not remedy the deficiencies of Yoon and Yang with respect to claim 19. Accordingly, Applicants respectfully submit that claim 19, and therefore claims 21-23 are allowable over the cited combination. Applicants respectfully request that the rejection of claims 21-23 be withdrawn and the claims allowed.

Claims 35, 38 and 41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam in view of Yang. This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 35 recites a method of "handling a plurality of semiconductor devices arrayed in a semiconductor wafer" including "adhering said semiconductor wafer to an integral flexible substrate, said integral flexible substrate comprising a plurality of ball grid arrays corresponding with said plurality of semiconductor devices," "connecting said semiconductor devices to respective ball grid arrays located on said integral flexible substrate," "testing said semiconductor devices through said ball grid arrays," and "subsequently, singulating packages from said semiconductor wafer and said integral flexible substrate, such that edges of each piece of said singulated semiconductor wafer and each piece of said singulated flexible substrate are aligned with each other."

As previously discussed, Lam relates to a wafer level packaging method which produces a stacked dual/multiple die integrated circuit package by attaching individual dies from a first wafer to each of individual dies on a second wafer and then singulating the second wafer to form the individual stacked-die IC packages. Yang relates to a wafer level package and the processing of the wafer level package including the steps of coating a wafer with an adhesive material, curing to harden the adhesive

material, and forming a plurality of pad openings in the adhesive material that are aligned to the pads of the dies.

Applicants respectfully submit that these references, whether considered alone or in combination, do not disclose all of the limitations of amended claim 35. Specifically, the references do not disclose, teach or suggest "adhering said semiconductor wafer to an integral flexible substrate, said integral flexible substrate comprising a plurality of ball grid arrays corresponding with said plurality of semiconductor devices," or "singulating packages from said semiconductor wafer and said integral flexible substrate, such that edges of each piece of said singulated semiconductor wafer and each piece of said singulated flexible substrate are aligned with each other."

Accordingly, Applicants respectfully submit that claim 35 is allowable over the cited combination. Claims 38 and 41 depend from claim 35 and are allowable along with claim 35. Applicants respectfully request that the rejection of claims 35, 38 and 41 be withdrawn and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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